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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,982	11/12/2003	Kai D. Feng	BUR920030142US1	2981

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EXAMINER	
NGUYEN, MINH T	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 03/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,982	FENG, KAI D.	
	Examiner	Art Unit	
	Minh Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-10 and 12-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-5,12-15 and 21* is/are rejected.

7)☒ Claim(s) *6-10,16-20 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2/14/05 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 2-5, 12-15 and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 6,222,402, issued to Boerstler et al.

As per claim 2, Boerstler discloses a PLL (column 4, lines 20-22, Fig. 4 is the charge pump for use with such an PLL), comprising:

a voltage controlled oscillator (column 4, lines 24-25, also see Fig. 1, VCO 5) for providing a first signal (Fig. 1, F0);

a phase comparator (Fig. 1, PFD 2, column 4, lines 29-32) for comparing the first signal (F0) to a reference signal (F_REF) and providing a control signal (UP and DOWN) representing a phase difference between the first signal and the reference signal (this is merely the function of any phase comparator); and

a charge pump circuit (Fig. 4) comprising a current source (NFET 36), a first FET (NFET 24), a second FET (NFET 26), a first capacitor (the capacitor which is connected to node VCB, see Fig. 1, capacitor C) wherein the first FET, second FET and first capacitor electrically coupled (as shown, they are electrically connected in the charge pump circuit 10), wherein the current source is directly connected to the source of the first FET (the current source which is NFET 36 is directly connected to the source of FET 24), wherein the current source is coupled between the source of the first FET and ground (FET 36 is between the source of FET 24 and GND), wherein the second FET comprises a parasitic capacitance (every FET has this element when the FET is operated in a switching environment), wherein the charge pump circuit is for receiving the control signal (UP and DOWN) and controlling the VCO such that a phase of the first signal equals a phase of the reference signal (any PLL performs this function), and wherein the second FET is adapted to be operated such that a spark current resulting from a switching mode of the control signal is directed through the parasitic capacitance to ground (Fig. 5, column 5, lines 46-54).

As per claim 3, the first FET (24) clearly receives the control signal (UP) at the gate, and since the first FET is an NFET, the functional recitation is met, i.e., ON at logic high and OFF at logic low.

As per claim 4, the recited limitation is met as shown in Fig. 5.

As per claim 5, the first (24) and second (26) FETs are clearly NFETs.

As per claim 12, the claim is merely a method to operate a PLL having the structure noted in claim 2, since Boerstler teaches the circuit, he inherently teaches the recited method.

As per claims 13-15, these claims are rejected for the same reasons noted in claims 3-5, respectively.

As per claim 21, since FETs 36 and 36 are configured as current mirror, the current through FET 36 is seen as constant, the recited limitation is met.

3. Claims 2-5, 12-15 and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,774,730, issued to Gasparik.

As per claim 2, Gasparik discloses a PLL (Fig. 3B is the charge pump for use with a PLL, for example, Fig. 1), comprising:

a voltage controlled oscillator (Fig. 1, the combination of VTI 106 and ICO 108) for providing a first signal (Fig. 1, FIO);

a phase comparator (Fig. 3B, PD 316) for comparing the first signal (FIO) to a reference signal (FIN) and providing a control signal (VEP and VEN) representing a phase difference between the first signal and the reference signal (this is merely the function of any phase comparator); and

a charge pump circuit (Fig. 3B) comprising a current source (NFET MN1 306), a first FET (NFET MN2A 356), a second FET (NFET MN2B 358), a first capacitor (capacitor CC) wherein the first FET, second FET and first capacitor electrically coupled (as shown, they are electrically connected in the charge pump circuit 350), wherein the current source is directly connected to the source of the first FET (as shown, the current source which is NFET MN1 306 is directly connected to the source of NFET MN2A 356), wherein the current source is coupled between the source of the first FET and ground (NFET MN1 306 is between the source of NFET MN2A 356 and GND), wherein the second FET comprises a parasitic capacitance (every FET has this element when the FET is operated in a switching environment), wherein the charge pump circuit is for receiving the control signal (VEP and VEN) and controlling the VCO such that a phase of the first signal equals a phase of the reference signal (any PLL performs this function), and wherein the second FET is adapted to be operated such that a spark current resulting from a switching mode of the control signal is directed through the parasitic capacitance to ground (column 5, lines 34-48).

As per claim 3, the first FET (MN2A 356) clearly receives the control signal (VEN) at the gate, and since the first FET is an NFET, the functional recitation is met, i.e., ON at logic high and OFF at logic low.

As per claim 4, the recited limitation is met as shown in Fig. 5.

As per claim 5, the first (MN2A) and second (MN2B) FETs are clearly NFETs.

As per claim 12, the claim is merely a method to operate a PLL having the structure noted in claim 2, since Gasparik teaches the circuit, he inherently teaches the recited method.

As per claims 13-15, these claims are rejected for the same reasons noted in claims 3-5, respectively.

As per claim 21, since FETs 314 and 306 are configured as current mirror, the current through FET 306 is seen as constant, the recited limitation is met.

Allowable Subject Matter

4. Claims 6-10, 16-20 and 22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 6-10 and 22 are allowable because the prior art of record fails to disclose or suggest the inclusion of a structure which causes the second FET to operate in saturation mode as recited in claim 6. The prior art of record, Boerstler and Gasparik as discussed above, both using differential pairs technique to eliminate the spark current, therefore, the second FET cannot be operated in saturation mode as required by the claim.

Claims 16-20 are allowable for the same reason noted in claim 6.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is **571-272-1748**. The examiner can normally be reached on Monday, Tuesday, Thursday, Friday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

3/18/05

Minh Nguyen
Primary Examiner
Art Unit 2816